Defence Science Journal, Vol. 70, No. 3, May 2020, pp. 272-277, DOI : 10.14429/dsj.70.15283

An Approach to Emulate and Validate the Effects of Single Event Upsets using the PREDICT FUTRE Hardware Integrated Framework

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ABSTRACT

Due to the advances in electronics design automation industry, worldwide, the integrated approach to model and emulate the single event effects due to cosmic radiation, in particular single event upsets or single event transients is gaining momentum. As of now, no integrated methodology to inject the fault in parallel to functional test vectors or to estimate the effects of radiation for a selected function in system on chip at design phase exists. In this paper, a framework, PRogrammable single Event effects Demonstrator for dIgital Chip Technologies (PREDICT) failure assessment for radiation effects is developed using a hardware platform and aided by genetic algorithms addressing all the above challenges. A case study is carried out to evaluate the frameworks capability to emulate the effects of radiation using the co-processor as design under test (DUT) function. Using the ML605 and Virtex-6 evaluation board for single and three particle simulations with the layered atmospheric conditions, the proposed framework consumes approximately 100 min and 300 min, respectively; it consumes 600 min for 3 particle random atmospheric conditions, using the 64 GB RAM, 64-bit operating system with 3.1 GHz processor based workstation. The framework output transforms the 4 MeVcm^2/mg linear energy transfer to a single event transient pulse width of 2 μs with 10^5 amplification factor for visualisation, which matches well with the existing experimental results data. Using the framework, the effects of radiation for the co-processing module are estimated during the design phase and the success rate of the DUT is found to be 48 per cent.

Keywords: Cosmic radiation; FPGA; Fault injection; Single event effects; Single event transients; Single event upset

1. INTRODUCTION

In spite of various advantages due to Moore's law i.e., reduction in die geometry due to shrinkage in transistor dimensions, the immunity level for the noise especially for cosmic radiation effects is reducing. Radiation hardening can be done at circuit level, design level and chip level. Radiation hardening can be done by design approach to mitigate the effects of single event upset (SEU) and single event transients (SET)[1].

Worldwide, the traditional radiation chamber method is used to analyse the effects of radiation on system on chip (SoC). Techniques for re-creating the single event effects (SEEs) during the design phase itself is limited and also to develop the mitigation techniques against radiation, considerable amount of effort in terms of time and cost is required. The approach using SEU tolerant design is used to mitigate the SEE effects in finite impulse response (FIR)[2]. To re-create the SEEs, researchers developed re-configurable FPGA based fault injection systems using memory re-configuration methods. A fault injection based comparison of dual modular redundancy and concurrent error detection in FIR filters is carried out in[3]. Soft error detection and correction based on C-element and bulk built-in current sensors (BICS) for radiation hardening is studied[4] and efficient implementation of 4-bit burst error correction for memories is presented in[5]. Worldwide the application of evolutionary algorithm viz., genetic algorithm based optimisation to solve complex design challenges using hardware approach is discussed in[6].

In this paper, a framework is proposed to emulate the effects of radiation for a digital SoC function during the design phase itself. The framework supports the feature to select the intensity of the SET pulse width depending on the input conditions.

2. BACKGROUND

The SEU phenomenon was first observed[7] and reported in a satellite system[8]. The soft errors due to alpha particles were observed with experimental methods[9]. The errors produced by sea level cosmic rays in computer memories were reported[10]. Effects of radiation with variation in altitude and shielding, various mission challenges and critical errors produced by cosmic ions in voyager and pioneer are discussed[11]. Hubble space telescope guidance system error which requires frequent scrubbing and Superbird Japanese satellite loss due to SEU and operator error are discussed[12]. Radiation hardened electronics for space exploration (RHESE) project was

Received : 12 December 2019, Revised : 13 March 2020
Accepted : 20 March 2020, Online published : 27 April 2020

conceived under various technology development initiatives planned in exploration technology development program (ETDP)[13] to achieve various objectives including human flights to lunar surface. The primary sources of radiation are trapped protons and electrons in earth's magnetic field, solar coronal mass ejections and galactic cosmic rays. The energy associated with these particles ranges from the lower level 1MeV to ~5 x 10^{19} MeV[14,15] by extremely energetic galactic cosmic rays. The particles between these energy levels have high probability to penetrate the material causing localised ionisation and probable atomic displacement termed as SEEs. The SEE is sub-classified into single event latch-up (SEL) and single event upset (SEU). Since SEL mitigation is carried out using process based solutions, focus was on SEU and SET analysis, simulation and modelling during the design phase.

The SEEs modelling involves knowledge of the environment in terms of particle flux and energy, penetration of charge into the layers and SET pulse width based on the linear energy transfer created due to the penetration length. Tools such as CREME86[16], MACREE[17] and SPENVIS[18] and other software modelling tools were developed to predict the SEE rates. All the above simulation methodologies are used for predicting the effect of radiation which translates to a single event upset. The radiation effect is modelled as faults and the same is injected into the DUT. Fault is injected in the design at various levels i.e., hardware, simulation and emulation. The hardware testing is carried out at actual radiation environment and simulation uses the HDL models and both need a tradeoff between accuracy, cost and time. The emulation method downloads the design and test vectors in a re-configurable platform, and upsets are modelled by toggling the configuration memory bits, which in turn creates faults in the flip-flops and gates in FPGAs. In this method, the failure mode analysis for a specific function and multiple fault injection for the dynamic environment variation, and limiting the number of injection points, while not disturbing the functional design (flip-flops and gates) are the prevailing challenges for failure analysis.

From the above literature survey, considering the limited availability of information in public domain and strong application potential for developing reliable design, it is evident that no emulation method which integrates the SEE simulation and translates the result in the form of SEUs and injects the same in a hardware platform to understand the effects in the design is available. In this paper, a framework addressing the challenges is designed with the integrated feature to inject the fault without disturbing the functional logic similar to the actual radiation environment is discussed.

3. ARCHITECTURE OF THE FRAMEWORK

Figure 1 shows the framework having three major sub-systems:

(a) The configuration and result analysis system
(b) FPGA based perturbation generator, controller, injector with arbiter algorithms and
(c) FPGA based DUT function to be analysed for SEEs.

A system clock is used for synchronisation between the modules. The input parameters for generating the perturbations and their associated functions are fed through the GUI based configuration system. Based on the configuration input, the particle simulation traces the interaction and movement of cosmic radiation with atmospheric molecules and computes the touch down velocity, hitting the SoC under observation.

The velocity, energy and angle of incidence of the high energy particle, degradation and composition variation in the atmospheric molecules were modelled as generic algebraic functions with a provision to integrate the user based function. The framework design flow with sub-modules is shown in Fig. 2. The configuration system transmits the inputs to the perturbation generation module to compute the particle simulation outputs such as LET, velocity and angle of particle hitting the surface volume (DUT). Perturbation controller generates the SET pulse width based on the particle simulation data shown in Fig. 2. The genetic algorithm generates the total number of faults, the corresponding nodes to inject the fault and the associated pulse width, which are shown in Fig. 2. The

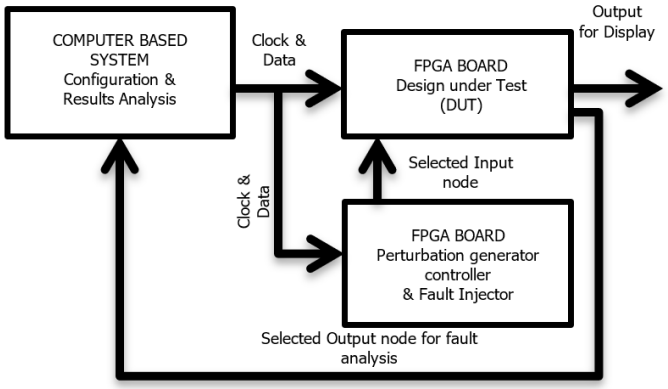


Figure 1. Architecture of the framework.

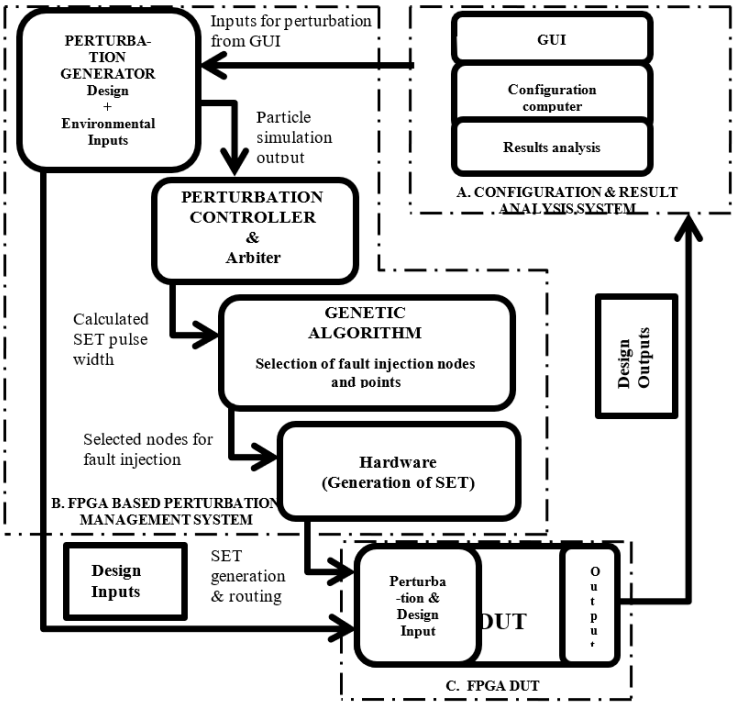


Figure 2. Design and sub-modules for the PREDICT framework.

pulse generated by the hardware is fed to the selected nodes in DUT. The selection of function to estimate the effects of radiation is carried out in the design phase. The outputs of the logics selected for fault tolerance assessments are brought to the top-level to store and analyse the response. The outputs are stored in the result analysis computer for analysis. Mathematical formulation used to calculate the peak and time duration of the SET pulse based on the input conditions is presented in the following section.

4. MATHEMATICAL FORMULATION AND FRAMEWORK DESIGN

Using the Genetic Algorithm (GA), the perturbation controller, generates the total number of faults for a particular set of input conditions and its corresponding nodes for injecting the same. The SET pulse (fault) width amplitude (V_{peak}) and duration (T_D) generated due to the radiation charge deposition are expressed as follows[19];

The peak amplitude V_{peak} of the SET is expressed as

$$V_{peak} = \frac{I_0 \tau_\alpha R}{\tau_\alpha - RC}\left(\left(\frac{\tau_\alpha}{RC}\right)^{RC/(RC-\tau_\alpha)} - \left(\frac{\tau_\alpha}{RC}\right)^{\tau_\alpha/(RC-\tau_\alpha)}\right) \quad (1)$$

where V_{peak} is the peak transient voltage, I_0 minimum charge collection current, τ_α collection time constant, R effective resistance of the pull-up-path, C effective capacitance loading lumped onto the output node.

The transient pulse duration width T_D is expressed as

$$T_D = t_{peak} - RC \ln\left(\frac{V_{DD}/2}{V_{peak}}\right) - \tau_\alpha \ln\left(\frac{V_{DD}/2}{V_{peak}}\right) \quad (2)$$

$$t_{peak} = \left(\frac{\ln(\tau_\alpha / RC)\tau_\alpha RC}{\tau_\alpha - RC}\right) \quad (3)$$

where V_{DD} is the supply voltage and t_{peak} instant the node voltage at its maximum. From Eqns. (1), (2), and (3), the transient pulse duration and pulse amplitude can be calculated.

It is impractical to understand a complex design thoroughly to develop the best case fault scenarios and the effect of simultaneous disturbance to simulate the failures. As such, in our proposed framework, the evolutionary algorithm based approach has been developed to create the realistic effect of the environment which also supports injection of faults (SET pulse) at the desired functional locations and predetermination of the injection instant in parallel. The GA is implemented to facilitate the trade-off between the requirement of computation resources and the complexity of maximum possible combinations. The GA computes the best group of faults and their locations in terms of nodes to inject the SET to obtain the worst failure combination based on the design requirements. During the design phase, the designer identifies the worst case scenario, for injecting the faults.

Subsequently, a test rule is generated by designers using the identified combinations. All the elements in the test rule are a set of combination of input nodes with a high probability of creating a fault in a specific function governed by designers. The algorithm compares the elements generated by GA and the test rule matrix and stores the result as total number of matched and non-matched elements. In the case of non-matched elements, the difference between the GA element and test rule matrix element is termed as effort. Ideally, the best case fault vector is the one with zero overall effort. The algorithm selects the fault sequence with the maximum matching nodes. The GA computes the best fault sequence using mutation, to generate the worst scenario. One of the mutation sequences extracted from the case study is explained in Table 1.

Table 1. Extract of the mutation sequence during the fault sequence generation using the GA flow

S. No.	The output generated by GA for fault simulation
1.	Total number of faults = 4
2.	F(1)
3.	Total number of nodes-5
4.	Node numbers:- 57 45 70 63 68
5.	Rule Matrix
6.	80 68 31 40 77 Matching = 0 Non-matching = 5 Eff[0]=-23 Eff[1]=-23 Eff[2] = 39 Eff[3] = 23 Eff[4] = - 9 effort = |7|
7.	Max No of matching = 1
8.	Matching rows:-
9.	47 45 79 99 35 effort:- |2|
10.	52 45 80 71 3 effort:- |52|
11.	81 98 70 93 73 effort:- |112|
12.	51 1 70 47 49 effort:- |84|
13.	The least effort is |2|
14.	The corresponding entry is :- 47 45 79 99 35 Effort = |2|

Based on the input conditions the GA generates four faults to be injected in the DUT as shown in Table 1 line 1. In the next step, the sub-function to inject one of the faults F(1) is generated using the random generator and environmental input conditions shown in Table 1 line 3. Subsequently, the algorithm generates input nodes for the sub-functions to inject the faults as shown in Table 1 line 4. The generated input nodes are compared with the test rule stored input nodes and effort is generated as shown in Table 1 line 6. Since none of the elements matched, the value zero is assigned to the matching variable. The algorithm searches for the nodes with the maximum number of matching elements. In this case, since the maximum matching elements between GA and test rule is one, the associated elements were used to compute the effort shown in Table 1 lines 7, 9, 10, 11, 12. The algorithm selects the elements with the least effort and stores as the best case worst node for mutation shown in Table 1 line 14. The pictorial representation of the SET generation using GA is shown in Fig. 3. The fitness evaluation function utilizes the non-matching element effort in mutation to generate the worst case fault for injecting it to the selected hardware nodes.

5. RESULTS AND DISCUSSION

A case study was presented with the results to evaluate the performance of the framework for the input conditions presented in Table 2. The case study DUT is a co-processing module used as an interface between the main processor and the actuation logic. The DUT processes, formats and transfers the data using a protocol and consumes 39 registers, 17 1-bit 2-to-1 multiplexers, 3 counters, 64x12 bit single port RAM in Xilinx XC6VLX240T FPGA. The particle simulation

Table 2. Input parameters

Parameter	Value	Parameter	Value
Altitude	100Km	TID	Upto 100 KRAD
Endurance	Upto 6 months	Energy reduction/hit & Velocity reduction/hit	Generic function
Exposed surface area	40 m × 40 m	Energy	100 MeV (at t_0 simulation)
Shielding	Nil (Worst case)	Velocity	3 x 10^8 m/s (at t_0 simulation)
Temperature/Pressure	-80 °C/0.001 mbar	Atmospheric composition	Nitrogen, Oxygen, Argon and Helium (equal concentration)

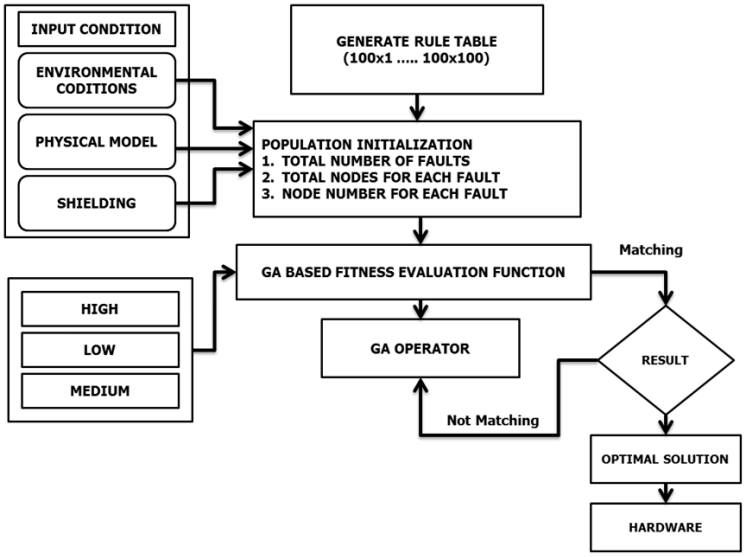


Figure 3. Pictorial representation of the SET generation using the GA flow.

computed the LET of the particle hitting the DUT, based on the movement of ions. The simulation is shown in Fig. 4 to visualise the particle movement. The *z*-axis defines the altitude. The *x* and *y* axes define the dimensions of the surface volume (DUT). Note that Fig. 4 visualises the two-particle simulation with scattered atmospheric molecules, red having the highest energy. A sum of 400 fault instances was generated and each fault instance had a maximum of 4 nodes. The FPGA hardware setup was used for injecting the fault using the touchdown LET value of 4 MeVcm^2/mg which generated the SET pulse of 2 µs with 10^5 visualisation amplification factor as shown in Fig. 5.

The ML605 evaluation board was used for hardware emulation. The FPGA used was Virtex-6 XC6VLX240T. The co-processing logic in the DUT was injected with an upset and the result was observed. For visualisation, one of the injected fault sub-function and its results are shown in Fig. 6. The golden (functional) output and the fault function (with SET) output are compared for every simulation clock cycle. The golden and the fault functional output matches before the fault injection point are highlighted in green window. After the fault injection (upset), the output differs which is highlighted in the red window. The results were captured with and without upset pulse and were compared for further analysis. The designer, based on the results, needs to improve the fault tolerance for a specific function. The SET pulse generated by the framework was compared with the experimental data[20]. The results proved that the characteristic of pulse width generated by the framework shown in Fig. 5 and experimental data match well. As briefed currently, no integrated methodology similar to the framework to inject the fault in parallel to functional test vectors or to estimate the effects of radiation for a selected

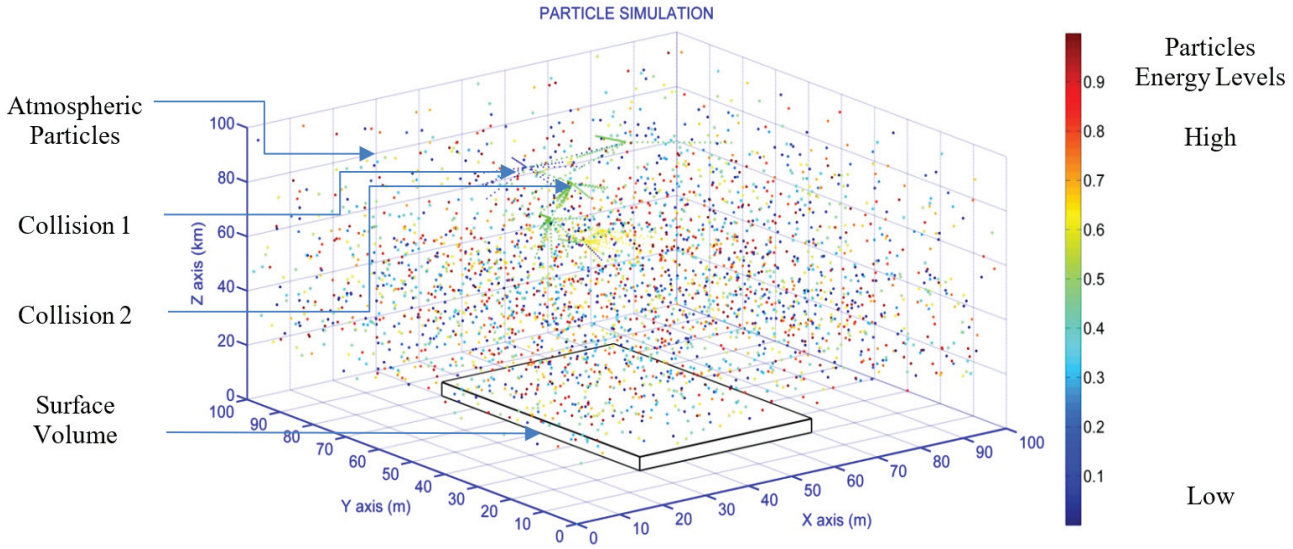


Figure 4. Modelling of the movement of ions collision with atmospheric composition using the particle simulation.

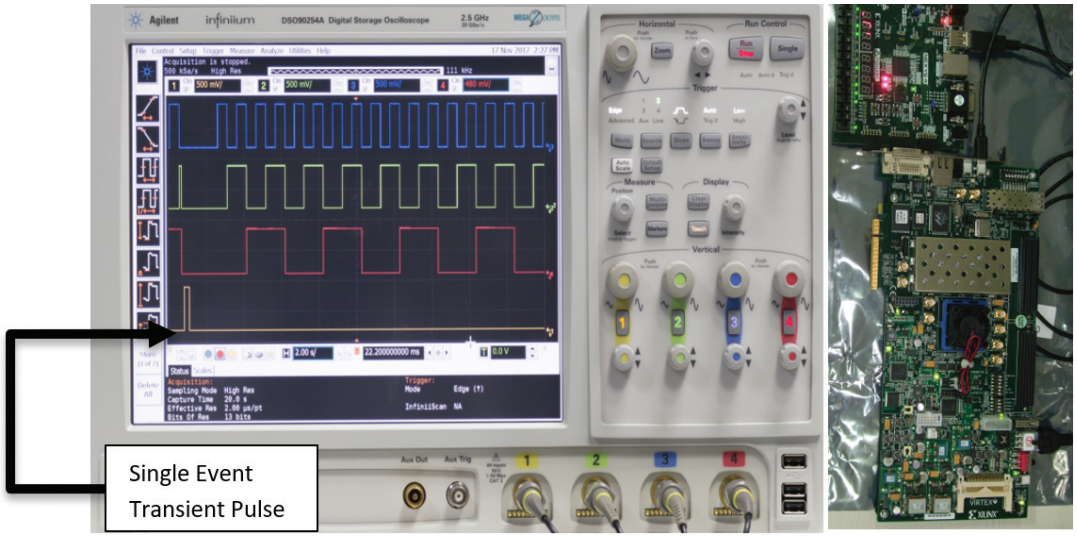


Figure 5. Emulation setup demonstrating the SET pulse generation using the framework.

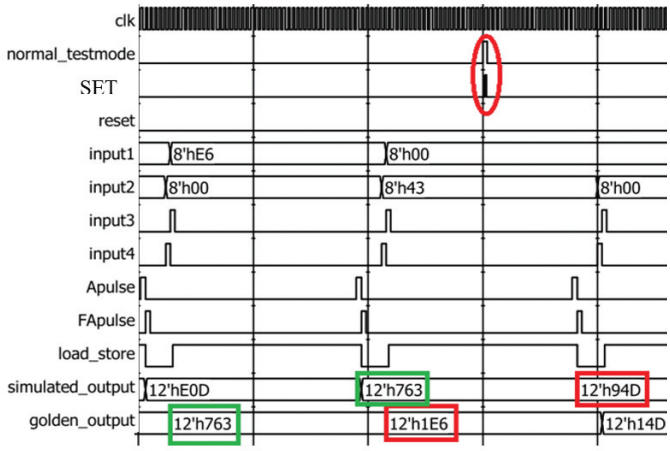
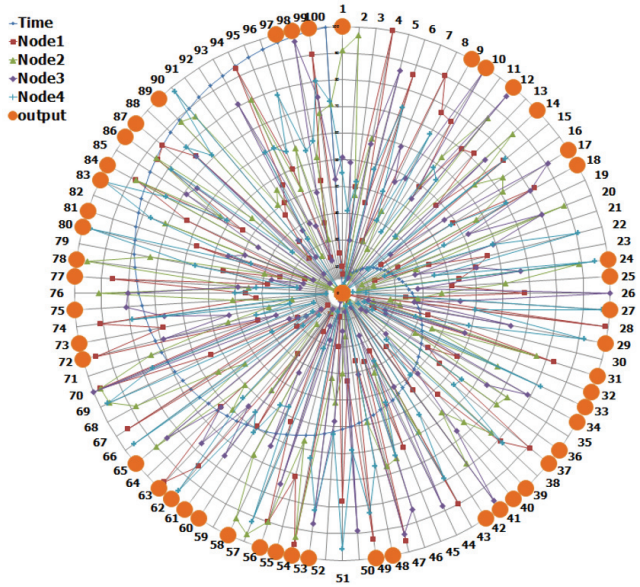


Figure 6. Results of the DUT before fault injection and after fault injection using the framework.

function in system on chip (SoC) at design phase exists. Using the framework, 400 faults were injected in the DUT in a step size of 10 ms functional cycle concurrent to the functional input. The overall success rate of DUT has been measured to be around 48 % which significantly impacts the overall functionality shown in radar graph in Fig. 7. The points on the outermost circle signify that the sub-function is passed for the particular instant of fault injection.



DUT Nodes subjected to test shown in the circumference = 100
Nodes passed ( ) = 48
Nodes failed ( ) = 52
DUT pass % = Passed/Total nodes = 48/100

Figure 7. Radar graph depicting the DUT result for 100 sub-functions.

6. CONCLUSION

In this paper, we have described the GA based emulation framework to inject the SET during the design phase. A case study and its results were also presented. The framework developed can generate and inject the faults based on the user radiation specifications in the design phase and without subjecting the chip to the actual radiation environment. Based on the input conditions the generated LET from the particle simulation produces a SET pulse, and GA propagates the pulse to the corresponding nodes for fault injection. The results proved that the characteristic of pulse width generated by the framework shown in Fig. 5 and experimental data match well. Using the framework, the designer can assess the effectiveness of reliability to develop appropriate mitigation techniques for a function during the design phase itself. The framework consumes a run time of 100 min, 300 min, and 600 min for single, three particles with layered and random atmospheric conditions respectively. The run time increases with nodes and with random atmospheric conditions. In future, it is planned to use a high performance computing platform to exercise the full potential of the framework with maximum nodes and random environment conditions to realise self-healing electronics architecture[21].

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ACKNOWLEDGMENTS

The author acknowledges the encouragement and support provided by Dr V. Natarajan, Director RIC & team to continue and pursue the research activity.

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He has significant contribution in research work outline, analysis of results and inputs for compilation of paper.