Template No. CEMILAC_SYSGP_SVR_18 SOFTWARE VERIFICATION REPORT for <LRU/SYSTEM Name> for <Platform Name>

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Amendment History

Issue	Issue Date	Brief	Change	Affected	Affected	Change Effective From
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		Amendment				
001		Initial Issue	NA	NA	NA	Initial
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1.0 INTRODUCTION

- 1.1 Purpose
- 1.2 Scope
- 1.3 Acronyms and Abbreviations
- **1.4 External Documents** Include references to standards, manuals, OEM documents etc.
- **1.5** Internal Documents

2.0 Verification Results

A complete description of the verification results generated at each activity of the software (application, system software, COTS components and PDIs) verification process as defined in the plans.

2.1 Software Planning Process Verification Results

Results of verification process/activities (Review/Analysis report along with closure of observations) carried out on the software planning phase documents including SCP/PSAC, SVP, SCMP, SDP, SQAP, Software Development Standards commensurate with software criticality level. Duly completed checklist of the activity may also be documented as part of SVR.

2.2 Software Requirement Process Verification Results

Results of verification process/activities (Review/Analysis report along with closure of observations) carried out on the software requirements documents/ data that are reviewed and analysed. The results may include the following: High level requirement correctness and completeness review, bi- directional traceability to system requirements, analysis of derived requirements, consistency within the requirements, compliance to requirements standards, compatibility with target computer hardware etc. Duly completed checklist of the activity may also be documented as part of SVR.

2.3 Software Design Process Verification Results

Results of verification process/activities (Review/Analysis report along with closure of observations) carried out on the Software Design phase documents. The results may include the following: Software architecture review, Low level requirement correctness and completeness checks, analysis of derived requirements, review of bi- directional traceability to high level requirements, algorithm verification results, bus load analysis,

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coupling analysis, complexity analysis, compliance to design standards etc. Duly completed checklist of the activity may also be documented as part of SVR.

2.4 Software Coding Process Verification Results

Results of verification process/activities (Review/Analysis report along with closure of observations) carried out on the source code. The results may include the following: Results of code walkthrough/review, traceability analysis, control & data coupling analysis for determinism, compliance to coding standard, robustness/ testability/ readability/ maintainability checks, no undocumented function implemented, stack usage, fixed point arithmetic overflow and resolution, resource contention, worst-case execution timing, exception handling, use of uninitialized variables or constants, unused variables or constants, and data corruption due to task or interrupt conflicts, Processor and memory load analysis, compatibility of processor architecture and hardware design to the code (Ex: size of int variable) etc., Duly completed checklist of the activity may also be documented as part of SVR.

2.5 Software Testing Process Verification Results

Results of verification process/activities (Review/Analysis/test report along with closure of observations) carried out on the software testing artefacts including test cases and results of: regression tests, low level testing, integration testing, HSI testing, system integration testing, aircraft integration testing etc. This may also include requirement based coverage analysis, normal and robustness test cases and results, external/ internal failure simulations, structural coverage analysis etc.

Configuration details of the test environment (hardware and software), testing and analysis tools, Test Rigs, supporting software etc. also to be documented.

3.0 Partitioning considerations

If partitioning is used, the verification results (review/analysis/test) that demonstrate the integrity of the partitioning protection mechanism.

4.0 Multi Core Usage

A verification of the configuration settings for multi core processors, verification results (review/analysis/test) for: robust resource partitioning and/or robust time partitioning, usage of shared interconnect, usage of dynamic features that are built into some MCPs, WCET of a software component or task when other software components or tasks are executing in parallel on the other cores of an MCP in the intended final configuration etc.

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5.0 Compiler configuration verification

Verification of correctness of compiler configuration settings made including the optimisation features.

6.0 Object Code Verification Results

Results of OCV activities performed may be documented.

7.0 Tool qualification Results

Results of tool qualification activities performed may be documented.

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