Template No.
CEMILAC_SYSGP _CFDR_04

CONSOLIDATED FIRMWARE DESIGN RECORD
for <LRU/SYSTEM Name>
for
<Platform Name>

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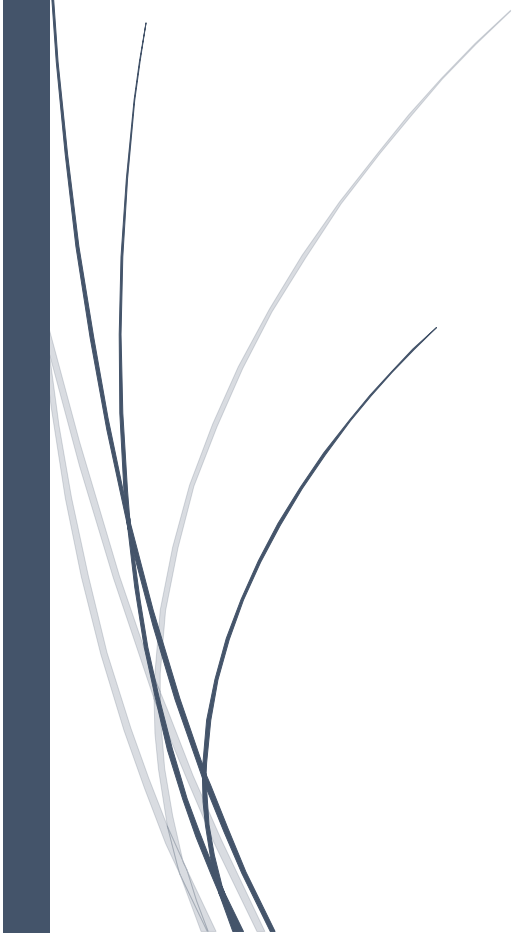

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Title:	**Project/System :**
CONSOLIDATED FIRMWARE DESIGN RECORD for <LRU/SYSTEM Name>for <Platform name>	< Project/System Name>
	LRU/System Part No.
	<No.>
	Critical Level
	<A/B/C/D/E>

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Disclaimer:

This document is a guidance document. Applicable section / table rows may be considered. Any additional details may be added. Any not applicable section/ table rows may be deleted. The template is very general and vary with process to process followed by Development Agency. The document may be fine-tuned with the TAA for finalization.

Contents

1. Introduction to the system
    a. Context diagram with overall system, LRU and FPGAs
    b. FPGA, make, type, Operating frequency, development environment, implementation language, verification tools

2. Requirements for FPGA implementation
    a. Coding/ design standards
    b. Interfaces and protocols to external devices with timing constraints
    c. Interaction between multiple programmable devices
    d. Functional requirements with modes of operation
    e. Finite state machine
    f. Failure detection and safety monitoring

3. Design details
    a. IP cores, if any
    b. Block diagrams
        i. List of basic (leaf) blocks and their functions
        ii. Component instantiations and wiring from basic blocks to top level
    c. Pin details , with named signal mapping
    d. Parameter definitions
    e. Clock and Reset configuration
    f. Memory mapping
    g. Timing diagrams
        i. Synchronous and sequential processes
        ii. Asynchronous and concurrent processes

4. Testing and verification
    a. Statement/ block coverage
    b. Requirement based testing at FPGA I/O level
    c. Gate-level net-list inspection
    d. Fault injection and corner case simulations
    e. Automatic regression testing, if any
    f. Worst and best case timing and clock skew analyses
    g. HDL (Hardware Design schematic-list) Simulation checks
    h. In circuit tests

5. Test sheet templates