Template No.
CEMILAC_SYSGP _CM_03

COMPLIANCE MATRIX FOR AIRBORNE STORE for <LRU/SYSTEM Name> for <Platform Name>

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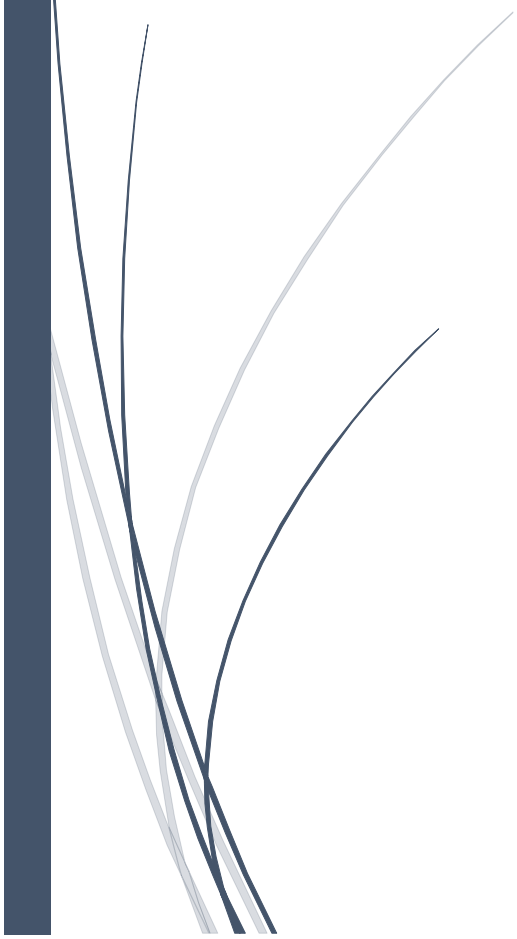

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Title:	**Project/System :**
COMPLIANCE MATRIX FOR AIRBORNE STORE for <LRU/SYSTEM Name>for <Platform name>	< Project/System Name>
	LRU/System Part No.
	<No.>
	Critical Level
	<A/B/C/D/E>

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Disclaimer:

This document is a guidance document. Applicable section / table rows may be considered. Any additional details may be added. Any not applicable section/ table rows may be deleted. The template is very general and vary with process to process followed by Development Agency. The document may be fine-tuned with the TAA for finalization.

mpliance Checklist for Airborne Stores

System Level

Sl.No.	Activity/ Document	Compliance	Remarks
1	Concept of Utilization		
2	FHA & SSA as per MIL-STD-882E and Common Cause Analysis as per ARP 4754A		
3	Functional/ System Requirement Document		
4	Inter-operability/ compatibility with co-located systems		
5	Test rigs and Simulators availability & certification		

Test Requirement Traceability Matrix

		Means of Compliance											
	Requirement	**Doc Ref (QTP/ACP/ Tech Spec/ MoM)**	**Review**	**Analysis**	**Simulation**	**Similarity**	**Product History**	**Inspection**	**Lab level Test**	**Rig / Aircraft level test**	**Flight test**	**Other**	**Compliance status**
Physical	Dimensions												
	Weight												
	Installation (Rack / Hard Mount)												
	Grounding/ shielding/ Bonding												
	Marking												
	Materials												
	Power Consumption												
	Connector pins												
	Insulation resistance												
	Leakage (Oil / Air / Nitrogen)												
Environmen	**Vibration** i) Sinusoidal ii) Platform specific iii) Buffet												

	iv) Acoustic Vibration v) Gun Fire Vibration												
	High Temperature i) Storage ii) Operation												
	Low Temperature i) Storage ii) Operation												
	Shock i) Functional ii) Crash Hazard iii) Transit Drop iv) Bench Handling v) Safety Drop vi) Service Drop												
	Acceleration i) Structural ii) Functional												
	CATH												
	Humidity												
	Altitude												
	Fungus												
	Rain drip												
	Immersion												
	Salt fog												

	Sand and dust												
	Solar radiation												
	Fluid Contamination												
	Fire Resistance												
	Deep Sea Penetration												
	Acoustic Vibration												
	Pyroshock												
	Transit drop												
	Safety Drop												
	Service Drop												
	Bench handling												
	Tropical Exposure												
	Air Exposure												
	Bump												
	Gun fire vibration												
	Hail impact												
	Rain Drip / Blowing rain												
	Fast Cook Off												
	Slow Cook Off												
	Bullet Impact												
	Fragment Impact												
	Sympathetic Detonation												

Power Supply	Distortion spectrum measurements												
	Power interruption (50 ms)												
	Emergency Operation (16V)												
	Engine ON operation (12V)												
	Polarity reversal												
	Normal steady state (Voltage / Frequency)												
	Abnormal steady state (Voltage / Frequency)												
	Normal transients (Voltage / Frequency)												
	Abnormal transients (Voltage / Frequency)												
	Phase Sequence												
	Phase Unbalance												
	Input Distortion												
	Amplitude Modulation												

	Frequency Modulation												
EMI/EMC	RE101												
	RE102												
	RE103												
	CE101												
	CE102												
	CE106												
	CS101												
	CS103												
	CS104												
	CS105												
	CS109												
	CS114												
	CS115												
	CS116												
	CS117 (ESD)												
	CS118 (Lightning)												
	RS101												
	RS103 (xyz V/m)												
	RS105												
	HERO												
Design Validation	GVT												
	Flutter Analysis												
	Pit Drop												
	Wind Tunnel												
	Structural Load												
	Phase Checks												

	Sign Checks												
	Sensor In Loop												
	Hardware In Loop												
	Power Budget Analysis												
	Derating Analysis												
	EMI/EMC Analysis												
	Temperature Analysis												
	Modal Analysis												
	Signal Integrity Analysis												
	Optical design analysis												
Technical Specification	External interface1												
	External interface2												
	External interface3												
	Spec1												
	Spec2												
	Spec3												
	Parameter1												
	Parameter2												

	Parameter3												
	Parameter4												
	Parameter5												
	Maintenance requirement (Calibration, pressurisation etc)												
	Endurance / Duty cycle												
	MTBF												
	MTTR												
	Technical Life												
	Calendar Life												

ACP Compliance:

Certification Milestone (Rig Int, A/c Int, DFT, User trials, Production, Modification etc)	ACP section	Compliance status	Waivers, if any (ref)	Remarks

Note 1: The above tables are indicative. The rows and columns that are not applicable to the project may be removed and any other relevant rows/ columns may be added as applicable to the project. All the tests/analyses/ certifications completed till date shall be indicated in the tables. Tables are to be prepared LRU-wise (indigenous and bought-out). For bought out items, the compliance as mentioned in the OEM documents shall be populated in the tables.

Note 2: All applicable rows as per QTP, Tech Spec and ACP shall be retained in the table even if the test/ analysis is currently not to be carried out and will be done in future.

Software

Sl No	Activity/ Artefact	Latest updated Doc/Report avl?	IV&V status	Document approval status	Remarks	PSAC Ref.
1	Software Certification Plan					
2	Software Requirement Document					
3	Software Requirement Review					
4	Software Design Document					
5	Software Design Review					
6	Algorithm Validation					
7	Source Code					
8	Code walkthrough report					
9	Software module/ CSCI/ HSI level Test cases					
10	Integration level test cases					
11	HILS test cases					
12	Bidirectional Traceability Matrix					
13	Static Analysis (memory, stack, bus load, coding standard, complexity, data/control coupling, sw & Hw architecture compatibility)					
14	Dynamic analysis (WCET, timing, coverage, exception handling, run time errors)					
15	Software Test Reports					
16	Version Description Document					

17	IV & V recommendations		NA			
18	SPR, SCR, SCN					
19	Test rig Software					

FPGA

Sl No	Activity/ Artefact	Latest updated Doc/Report avl?	IV&V status	Document approval status	Remarks	PHAC Ref
1	Hardware Certification Plan					
2	Hardware Requirement Document					
3	Hardware Requirement Review					
4	Hierarchical schematics, Block diagrams, Floor planning					
5	Hardware Design Review					
6	Algorithm Validation					
7	VHDL Code, RTL code, Finite State machine					
8	Code walkthrough report					
9	In-circuit test cases					
10	Netlist, Synthesis report, Place and Route report					
11	Elemental analysis/ Code coverage					
12	Timing and clock skew analysis, Logic analysis, resource analysis					
13	Functional failure path analysis, common mode failure analysis					
14	Pin details with signal mapping					
15	In target at speed Test Report					
16	IV&V recommendations		NA			

17	Version Description Document					
18	PRs and CNs					
19	Test rig software					