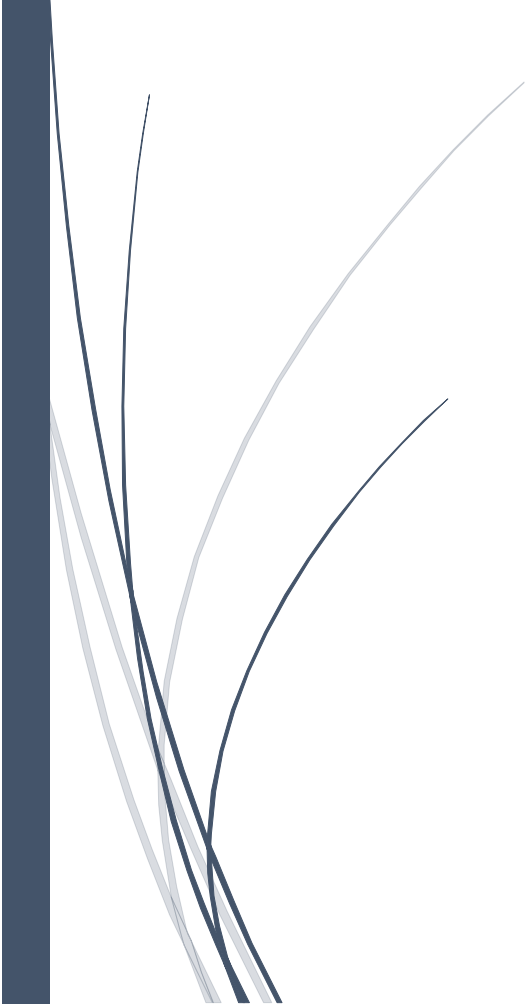


Compliance Matrix for Air Launched Weapon

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Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 2 of 15

Disclaimer:

This document is a guidance document. Applicable section / table rows may be considered. Any additional details may be added. Any not applicable section/ table rows may be deleted. The template is very general and vary with process to process followed by Development Agency. The document may be fine-tuned with the TAA for finalization.

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
				Page No: 3 of 15	

Compliance Checklist for Air Launched Weapons

System Level

Sl.No.	Activity/ Document	Compliance	Remarks
1	CONOPS		
2	System Safety Analysis/ Functional Hazard Analysis		
3	Product Breakdown Structure		
4	Functional/ System Requirement Document		
5	Test Requirement Traceability Matrix		
6	Inter-operability with co-located systems		
7	Test rigs and Simulators availability		

Product Breakdown Structure

Sl.No	Subsystem Name & Part Number :				Software		Firmware/ FPGA		IP Cores	
	Design agency	Realisation/ development agency	Govt QA agency	Part No.	Design agency	IV&V agency	Design agency	IV&V agency	Design agency	IV&V agency

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 4 of 15

Functional Hazard Analysis :

- a. Decomposition of the system and its related subsystems to the major component level.
- b. A functional description of each subsystem and component identified.
- c. A functional description of interfaces between subsystems and components. Interfaces should be assessed in terms of connectivity and functional inputs and outputs.
- d. Hazards associated with loss of function, degraded function or malfunction, or functioning out of time or out of sequence for the subsystems, components, and interfaces. The list of hazards should consider the next effect in a possible mishap sequence and the final mishap outcome.
- e. An assessment of the risk associated with each identified failure of a function, subsystem, or component. Estimate severity, probability, and Risk Assessment Code (RAC)
- f. An assessment of whether the functions identified are to be implemented in the design hardware, software, or human control interfaces. This assessment should map the functions to their implementing hardware or software components. Functions allocated to software should be mapped to the lowest level of technical design or configuration item prior to coding (e.g., implementing modules or use cases).
- g. An assessment of Software Control Category (SCC) for each Safety-significant Software Function (SSSF). Assign a Software Criticality Index (SwCI) for each SSSF mapped to the software design architecture.
- h. A list of requirements and constraints (to be included in the specifications) that, when successfully implemented, will eliminate the hazard or reduce the risk. These requirements could be in the form of fault tolerance, detection, isolation, annunciation, or recovery.

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 5 of 15

Sl.No	ID	Function	Hazard	Hazard Consequence	Final mishap/ outcome	Severity	Probability	Risk Assessment Code (RAC)	Implemented in	SwCI/ HwCI	Mitigation Requirements
1											
2											
3											

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 6 of 15

Test Requirement Traceability Matrix

		Means of Compliance									
	Requirement	Review	Analysis	Simulation	Equivalence	Product History	Lab level Test	Rig / Aircraft level test	Flight test	Other	Compliance status
Physical	Dimensions										
	Weight										
	Installation										
	Grounding/ shielding/ Bonding										
	Marking										
	Materials										
	Power Consumption										
Environmental	Vibration i) Sinusoidal ii) Platform specific iii) Buffet										
	High Temperature i) Storage ii) Operation										
	Low Temperature i) Storage ii) Operation										
	Shock										
	Acceleration i) Structural ii) Functional										
	CATH										

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 7 of 15

	Humidity										
	Altitude										
	Fungus										
	Rain drip										
	Immersion										
	Salt fog										
	Sand and dust										
	Solar radiation										
	Acoustic Vibration										
	Pyroshock										
	Transit drop										
	Safety Drop										
	Service Drop										
	Bench handling										
	Tropical Exposure										
	Air Exposure										
	Bump										
	Gun fire vibration										
	Hail impact										
	Blowing rain										
	Fast Cook Off										
	Slow Cook Off										
	Bullet Impact										
	Fragment Impact										
	Sympathetic Detonation										
PO	Distortion spectrum measurements										

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 8 of 15

	Power interruption (50 ms)										
	Emergency Operation (16V)										
	Engine ON operation (12V)										
	Polarity reversal										
	Normal steady state										
	Abnormal steady state										
	Normal transients										
	Abnormal transients										
EMI/EMC	RE101										
	RE102										
	RE103										
	CE101										
	CE102										
	CE106										
	CS101										
	CS103										
	CS104										
	CS105										
	CS109										
	CS114										
	CS115										
	CS116										
	CS117 (ESD)										
	CS118 (Lightning)										

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 9 of 15

	RS101										
	RS103 (xyz V/m)										
	RS105										
	HERO										
Design Validation	GVT										
	Flutter Analysis										
	Pit Drop										
	Wind Tunnel										
	Structural Load										
	Phase Checks										
	Sign Checks										
	Sensor In Loop										
	Hardware In Loop										
Technical Specification	External interface1										
	External interface2										
	External interface3										
	Spec1										
	Spec2										
	Spec3										
	Parameter1										
	Parameter2										
	Parameter3										
	Parameter4										
	Parameter5										

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 10 of 15

	Maintenance requirement (Calibration, pressurisation etc)										
	Technical Life										
	Calendar Life										

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 11 of 15

Software

SI No	Activity/ Artefact	Doc/Report avl?	IV&V Observations avl?	Observations closed?	Remarks
1	Software Certification Plan				
2	Software Requirement Document				
3	Software Requirement Review				
4	Software Design Document				
5	Software Design Review				
6	Algorithm Validation				
7	Source Code				
8	Code walkthrough report				
9	Software HSI level Test cases				
10	Integration level test cases				
11	HILS test cases				
12	Bidirectional Traceability Matrix				
13	Static Analysis (memory, stack, bus load, coding standard)				
14	Dynamic analysis (WCET, timing, coverage, exception handling)				
15	Software Test Reports				
16	Version Description Document				
17	IV & V recommendations		NA	NA	
18	SPR, SCR, SCN				
19	Test rig Software				

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 12 of 15

FPGA

SI No	Activity/ Artefact	Doc/Report avl?	IV&V Observations avl?	Observations closed?	Remarks
1	Hardware Certification Plan				
2	Hardware Requirement Document				
3	Hardware Requirement Review				
4	Hierarchical schematics, Block diagrams, Floor planning				
5	Hardware Design Review				
6	Algorithm Validation				
7	VHDL Code, RTL code, Finite State machine				
8	Code walkthrough report				
9	In-circuit test cases				
10	Netlist, Synthesis report, Place and Route report				
11	Elemental analysis/ Code coverage				
12	Timing and clock skew analysis, Logic analysis, resource analysis				
13	Functional failure path analysis, common mode failure analysis				
14	Pin details with signal mapping				
15	In target at speed Test Report				
16	IV&V recommendations		NA	NA	
17	Version Description Document				
18	PRs and CNs				
19	Test rig software				

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 13 of 15

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 14 of 15

Limitations:

Sl.No	Limitation/ Observation/Deviation	Operational and/or safety Implications of the limitation	Mitigation Plan	PDC for implementation of mitigation

Prepared By	Checked By	Approved By	Doc No. <Document number		
			Issue	Revision	Date
					Page No: 15 of 15